AMENDMENTS TO THE SPECIFICATION:

Kindly replace the paragraph beginning on page 14, line 23, with the following amended paragraph:

As described above, according to the first embodiment, the scanned information storing SRAM 22 is provided in the backup power supply region 19 of the LSI chip 1, and connected through the scan path 21 to the memory units 20 of the CPU 11, the CPU peripheral circuit 12, and so on in the main power supply region 18. When the system is placed in an operation standby state, information held in the memory unit 20 of the CPU 11 or the like is read through the scan path 21, and saved in the ~~built-in~~ scanned information storing SRAM ~~15~~ 22. When the system is returned from the standby state, the information stored in the scanned information storing SRAM 22 is set through the scan path 21 in the original memory unit 20 of the CPU 11 or the like. Thus, it is possible to realize a leakage current reducing method of an LSI capable of carrying out information saving and returning by a relatively simple switching operation without needing any special switching operations by the CPU 11, and resuming the operation immediately after the change to the standby state. Moreover, this method is capable of easily saving even information not memory-mapped in the address of the CPU 11.